CLAIMS

What is claimed is:

1. A method of automatically configuring media connections when operating in forced speed and duplex mode, the method comprising:

connecting a first pair of connectors to a first pair of conductors and a second pair of connectors to a second pair of conductors during a first state, and connecting the first pair of connectors to the second pair of conductors and the second pair of connectors to the first pair of conductors during a second state;

holding the first state or the second state if operating in forced speed and duplex mode, a defined time has not expired and another end of a link can receive a signal.

2. The method of claim 1 wherein the defined time is approximately four (4) seconds.

3. The method of claim 1, wherein Normal Link Pulses (NLPs) are transmitted during the defined time.

4. The method of claim 1, wherein an IDLE signal is transmitted during the defined time.

5. The method of claim 1, further comprising:

preventing a transition between the first state and the second state when a transmission is occurring in the link as indicated by a T_pulse signal.

6. An article of manufacture, comprising:

a machine-readable medium having stored thereon instructions to:

connect a first pair of connectors to a first pair of conductors and a second pair of connectors to a second pair of conductors during a first state, and connect the first pair of connectors to the second pair of conductors and the second pair of connectors to the first pair of conductors during a second state; and

hold the first state or the second state if operating in forced speed and duplex mode, a defined time has not expired and another end of a link can receive a signal.

7. A method of using an existing auto-MDI/MDIX function when operating in forced speed and duplex mode, the method comprising:

setting a chip into an auto-negotiation mode, and advertising a desired state;

performing the auto-MDI/MDIX function;

when a link is up, reading an MDI/MDIX state from a status register, where the MDI/MDIX state indicates the state of the other end of the link;

dropping the link;

forcing the MDI/MDIX state to the state found in the status register; and

forcing the speed and duplex mode.

8. An apparatus for automatically configuring media connections when operating in forced speed and duplex mode, the apparatus comprising:

means for connecting a first pair of connectors to a first pair of conductors and a second pair of connectors to a second pair of conductors during a first state, and connecting

the first pair of connectors to the second pair of conductors and the second pair of connectors to the first pair of conductors during a second state;

coupled to the connecting means, means for holding the first state or the second state if operating in forced speed and duplex mode, a defined time has not expired and another end of a link can receive a signal.

9. An apparatus for automatically configuring media connections when operating in forced speed and duplex mode, the apparatus comprising:

a media switch configured to connect a first pair of connectors to a first pair of conductors and a second pair of connectors to a second pair of conductors during a first state, and to connect the first pair of connectors to the second pair of conductors and the second pair of connectors to the first pair of conductors during a second state; and

a processor coupled to the media switch and configured to hold the first state or the second state if operating in forced speed and duplex mode, a defined time has not expired and another end of a link can receive a signal.

10. The apparatus of claim 9, further comprising:

a scrambler coupled to the processor and configured to generate an output for use by the processor to determine a transition between the first state and the second state.

11. The apparatus of claim 11, wherein the scrambler is an 11 bit shift register.

12. The apparatus of claim 9, wherein the processor includes a signal detector to detect if the other end of the link can receive a signal.

13. The apparatus of claim 9, further comprising:

a reset signal generator coupled to the processor and configured to reset the state to the first state.

14. The apparatus of claim 9, wherein the defined time is approximately four (4) seconds.

15. The apparatus of claim 9, wherein Normal Link Pulses (NLPs) are transmitted during the defined time.

16. The apparatus of claim 9, wherein an IDLE signal is transmitted during the defined time.

17. The apparatus of claim 9, wherein the processor is configured to prevent a transition between the first state and the second state when a transmission is occurring in the link as indicated by a T_pulse signal.

18. An apparatus for using an existing auto-MDI/MDIX function when operating in forced speed and duplex mode, the apparatus comprising:

means for setting a chip into an auto-negotiation mode, and for advertising a desired state;

coupled to the means for setting and for advertising, means for performing the auto-MDI/MDIX function;

coupled to the performing means, means for reading a MDI/MDIX state from a status register, where the MDI/MDIX state indicates the state of the other end of the link when a link is up;

coupled to the reading means, means for dropping the link;

coupled to the dropping means, means for forcing the MDI/MDIX state to the state found in the status register; and

coupled to the means for forcing the MDI/MDIX state, means for forcing the speed and duplex mode.

19. An article of manufacture, comprising:

a machine-readable medium having stored thereon instructions to:

set a chip into an auto-negotiation mode, and advertise a desired state;

perform the auto-MDI/MDIX function;

when a link is up, read an MDI/MDIX state from a status register, where the MDI/MDIX state indicates the state of the other end of the link;

drop the link;

force the MDI/MDIX state to the state found in the status register; and

force the speed and duplex mode.

20. An apparatus for using an existing auto-MDI/MDIX function when operating in forced speed and duplex mode, the apparatus comprising:

a processor configured to execute software to enable a method comprising:

setting a chip into an auto-negotiation mode, and advertising a desired state;

performing the auto-MDI/MDIX function;

when a link is up, reading an MDI/MDIX state from a status register, where the MDI/MDIX state indicates the state of the other end of the link;

dropping the link;

forcing the MDI/MDIX state to the state found in the status register; and

forcing the speed and duplex mode.